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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/851,471 | 05/07/2001 | Tzueng-Yau Lin | 81842.0005 | 3597 |

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| EXAMINER | |
|---|---|
| GIESY, ADAM | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2656 | |

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/851,471 | LIN, TZUENG-YAU | |
| | Examiner | Art Unit | |
| | Adam R. Giesy | 2656 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/[illegible]/01 & 12/23/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

2. Claims 7, 12, and 16 are objected to because of the following informalities:

Examiner asserts that the term 'MLP' should read 'Meridian Lossless Packing ® (MLP)'.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Craven et al. (hereinafter Craven – US Pat. No. 6,611,212 B1) in view of Fujinami (US Pat. No. 5,933,398).

Regarding claim 1, Craven discloses a playback system, comprising: a depacketizer circuit coupled to receive packets of audio data from a storage device, the depacketizer circuit extracting data and outputting one or more data streams (see Figure 2 – note element labeled 'DE-PACKETIZER' and that the element outputs substream 0 and substream 1); and at least one decoder core receiving the one or more data streams, the decoder decoding audio data according to a lossless unpacking scheme, wherein the depacketizer circuit and the at least one decoder core are coupled (Figure 2 – note elements labeled 'DECODER CORE 0' and 'DECODER CORE 1' are coupled to the DE-PACKETIZER through the FIFO buffers). Craven fails to disclose that the depacketizer provides data directly to the decoder without buffering.

Fujinami discloses a reproducing apparatus that decodes data wherein a decoder (Figure 1, element 5) separates the audio packet data (see column 7, line 66 thru column 8, line 5) and passes it directly to audio decoders (see Figure 1, elements 8a, 8b, and 8c) without passing through a buffer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the playback system as disclosed by Craven with the direct decoder-to-decoder circuit as disclosed by Fujinami, the motivation being to allow for real-time decoding of audio information without the need to buffer.

Regarding claim 2, Craven and Fujinami disclose all of the limitations of claim 1 as discussed in the claim 1 rejection above. Craven further discloses a matrixing circuit for generating at least partially correlated audio output from three or more streams from the at least one decoder core (Figure 2 – note element labeled 'INVERSE MATRIX 1').

Regarding claim 3, Craven and Fujinami disclose all of the limitations of claim 1 as discussed in the claim 1 rejection above. Craven further discloses that the at least one decoder core is two decoder cores, one decoder core receiving from the depacketizer circuit a substream comprising at least one audio channel, a second decoder core receiving from the depacketizer circuit a substream comprising up to four audio channels (Figure 2 – note elements labeled 'DECODER CORE 0' and 'DECODER CORE 1' as well as the substreams labeled m0-m5).

Regarding claim 4, Craven and Fujinami disclose all of the limitations of claim 3 as discussed in the claim 3 rejection above. Craven further discloses that the storage device is a DVD-Audio disk (see column 6, lines 1-13).

Regarding claim 5, Craven and Fujinami disclose all of the limitations of claim 3 as discussed in the claim 3 rejection above. Craven further discloses that the storage device is an optical storage disk (see column 6, lines 1-13).

Regarding claim 6, Craven and Fujinami disclose all of the limitations of claim 3 as discussed in the claim 3 rejection above. Examiner takes Official Notice that it is well known in the art to implement a communications link between a data store and the depacketizer circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the playback system as disclosed

by the combination of Craven and Fujinami with the communications link, the motivation being to make the circuit more versatile with different forms of signal input and output.

Regarding claim 7, Craven and Fujinami disclose all of the limitations of claim 1 as discussed in the claim 1 rejection above. Craven further discloses that the at least one decoder core performs MLP decoding on data read from a DVD (column 3, lines 40-45).

Regarding claim 8, Craven discloses a playback system, comprising: a depacketizer provided to receive packets of audio data from a storage device, the depacketizer extracting data and outputting one or more data streams (see Figure 2 – note element labeled 'DE-PACKETIZER' and that the element outputs substream 0 and substream 1); and at least one decoder core receiving the one or more data streams, the decoder decoding audio data, wherein the depacketizer and the at least one decoder core are defined within a digital signal processor (Figure 2 – note elements labeled 'DECODER CORE 0' and 'DECODER CORE 1'; see also column 23, lines 47-65 – this passage discloses that the circuit can be implemented in a processor). Craven fails to disclose that the depacketizer provides data directly to the decoder.

Fujinami discloses a reproducing apparatus that decodes data wherein a decoder (Figure 1, element 5) separates the audio packet data (see column 7, line 66 thru column 8, line 5) and passes it directly to audio decoders (see Figure 1, elements 8a, 8b, and 8c).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the playback system as disclosed by Craven with the

direct decoder-to-decoder circuit as disclosed by Fujinami, the motivation being to allow for real-time decoding of audio information without the need to buffer.

Regarding claim 9, Craven and Fujinami disclose all of the limitations of claim 8 as discussed in the claim 8 rejection above. Craven further discloses a matrixing circuit for generating at least partially correlated audio output from three or more streams from the at least one decoder core (Figure 2 – note element labeled 'INVERSE MATRIX 1').

Regarding claim 10, Craven and Fujinami disclose all of the limitations of claim 9 as discussed in the claim 9 rejection above. Craven further discloses that the matrixing circuit is implemented in the digital signal processor (column 23, lines 47-65).

Regarding claim 11, Craven and Fujinami disclose all of the limitations of claim 9 as discussed in the claim 9 rejection above. Craven further discloses a matrixing circuit for generating multichannel audio data (column 6, lines 35-67), the matrixing circuit implemented within the digital signal processor (column 23, lines 47-65).

Regarding claim 12, Craven and Fujinami disclose all of the limitations of claim 11 as discussed in the claim 11 rejection above. Craven further discloses that the at least one decoder core performs MLP decoding (column 3, lines 40-45).

Regarding claim 13, Craven and Fujinami disclose all of the limitations of claim 8 as discussed in the claim 8 rejection above. Craven further discloses that the at least one decoder core comprises first and second decoder cores (Figure 2 – note elements labeled 'DECODER CORE 0' and 'DECODER CORE 1'), the depacketizer providing a substream 0 to the first decoder core and providing a substream 1 to the second decoder core (see Figure 2 – note that substream 0 and substream 1 are provided to

decoder core 0 and decoder core 1, respectively, even though they first pass through FIFO buffers).

Regarding claim 14, Craven and Fujinami disclose all of the limitations of claim 13 as discussed in the claim 13 rejection above. Craven further discloses a matrixing circuit for generating multichannel audio data (column 6, lines 35-67), the matrixing circuit implemented within the digital signal processor (column 23, lines 47-65).

Regarding claim 15, Craven and Fujinami disclose all of the limitations of claim 8 as discussed in the claim 8 rejection above. Examiner takes Official Notice that it is well known in the art to implement a data transfer rate of 14.75 Mb/sec between the depacketizer and the at least one decoder core. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the playback system as disclosed by the combination of Craven and Fujinami with the data transfer rate of 14.75 Mbps, as per the maximum IDCS bus speed standard, the motivation being to enable the circuit to function with a high data transfer rate during real time operation.

Regarding claim 16, Craven discloses an MLP encoding system, comprising: a matrix circuit receiving a plurality of audio signal channels (Figure 1 – note element labeled 'MATRIX 1'); a first and second encoder core receiving data from the matrix circuit (note elements labeled 'ENCODER CORE 0' and 'ENCODER CORE 1'), the first and second encoders implementing MLP encoding on data output by the matrix circuit (see column 3, lines 40-65); a packetizer receiving first and second data substreams from the first and second encoders, respectively, and formatting audio data into packets

for storage on a storage medium, wherein the packetizer circuit and the first and second encoder cores are coupled (Figure 1 – note elements labeled 'ENCODER CORE 0' and 'ENCODER CORE 1' are coupled to the 'PACKETIZER' through the 'FIFO BUFFERS'). Craven fails to disclose that the depacketizer provides data directly to the decoder without buffering.

Fujinami discloses an apparatus that for signal manipulation wherein a decoder (Figure 1, element 5) manipulates audio packet data (see column 7, line 66 thru column 8, line 5) and passes it directly to audio decoders (see Figure 1, elements 8a, 8b, and 8c) without passing through a buffer.

It is the Examiner's position that the circuit as disclosed by Fujinami would function in reverse if the decoders were replaced by encoders with the proper set-up as demonstrated by the circuit as disclosed by Craven (figures 1 and 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the encoding system as disclosed by Craven with the direct encoder-to-encoder circuit as disclosed by Fujinami, the motivation being to allow for real-time encoding of audio information without the need to buffer.

Regarding claim 17, Craven and Fujinami disclose all of the limitations of claim 16 as discussed in the claim 16 rejection above. Examiner takes Official Notice that it is well known in the art to implement a data transfer rate of 14.75 Mb/sec between the depacketizer and the at least one decoder core. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the encoding system as disclosed by the combination of Craven and Fujinami with the data

transfer rate of 14.75 Mbps, as per the maximum IDCS bus speed standard, the motivation being to enable the circuit to function with a high data transfer rate during real time operation.

***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adam R. Giesy whose telephone number is (571) 272-7555. The examiner can normally be reached on 8:00am- 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne R. Young can be reached on (571) 272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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